

10

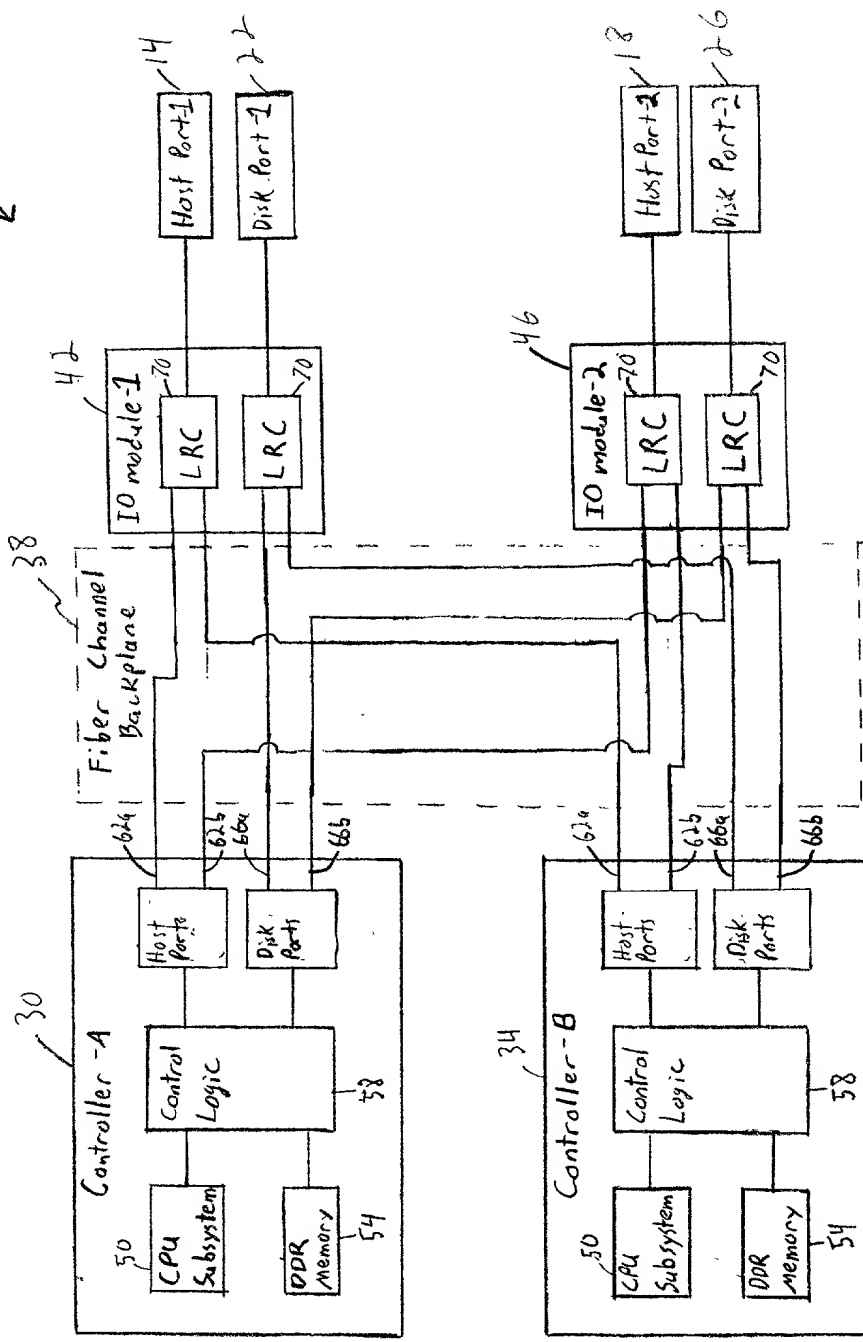


Fig. 1 (Prior Art)

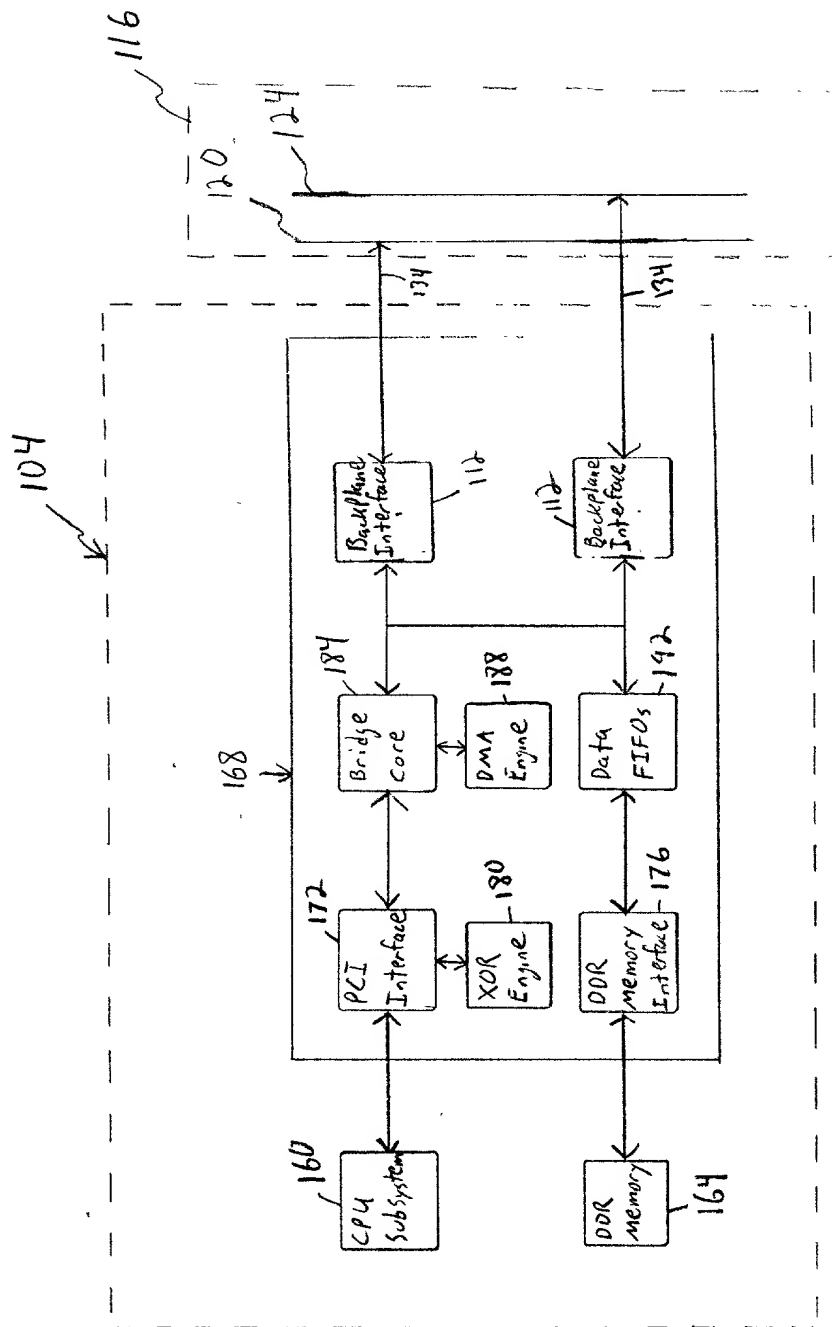


Fig 3

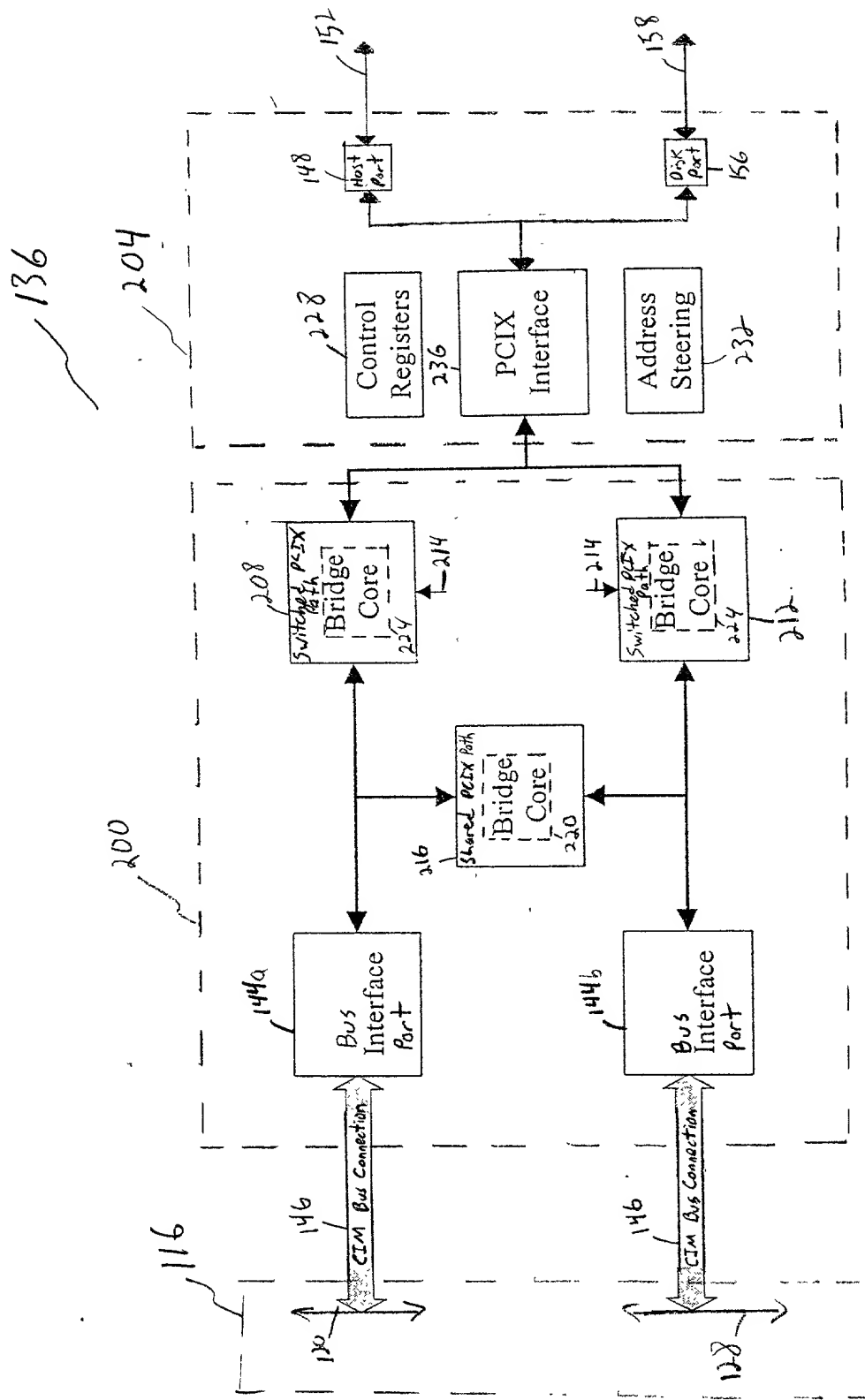


Fig. 4

FIG. 5 is a block diagram of a system 100a, including a backplane 116, a first module 104, a second module 108, a first controller module 136, and a second controller module 140. The first module 104 includes a CPU Subsystem 160, DDR Memory 164, and an Itchy Chicken 168. The second module 108 includes a CPU Subsystem 160, DDR Memory 164, and an Itchy Chicken 168. The first controller module 136 includes a Shared PCIX 216, Switched PCIX 212, and a Dual Port FC 204. The second controller module 140 includes a Shared PCIX 216, Switched PCIX 212, and a Dual Port FC 204. The backplane 116 includes four PCIX lanes: PCIX-A1, PCIX-A2, PCIX-B1, and PCIX-B2. The first module 104 is connected to the backplane 116 via PCIX-A1 and PCIX-A2. The second module 108 is connected to the backplane 116 via PCIX-B1 and PCIX-B2. The first controller module 136 is connected to the backplane 116 via PCIX-A1 and PCIX-A2. The second controller module 140 is connected to the backplane 116 via PCIX-B1 and PCIX-B2. The first controller module 136 is also connected to a Dual Port FC 204, which is connected to two external ports 152 and 158. The second controller module 140 is also connected to a Dual Port FC 204, which is connected to two external ports 152 and 158.

100a

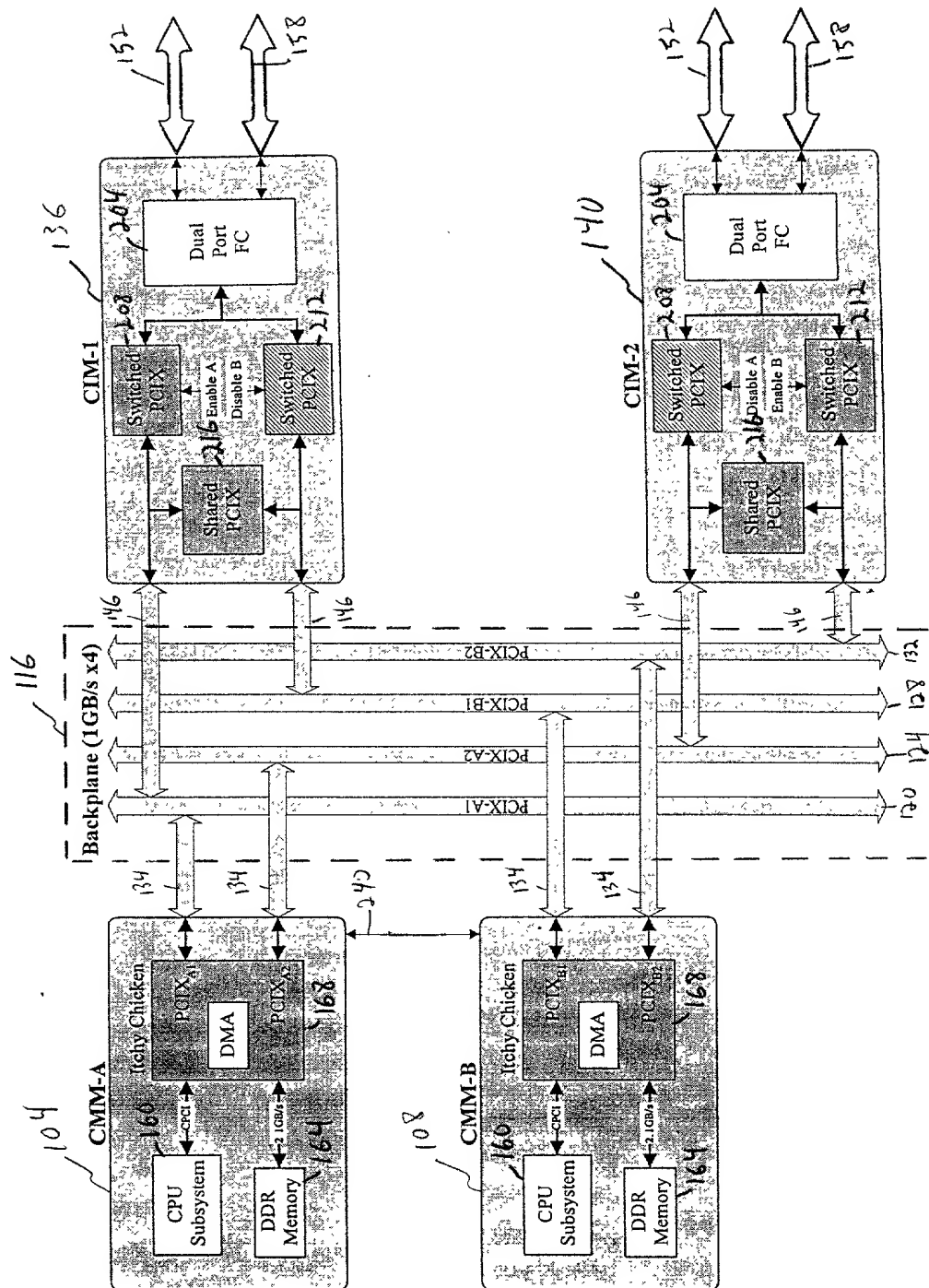


Fig 5

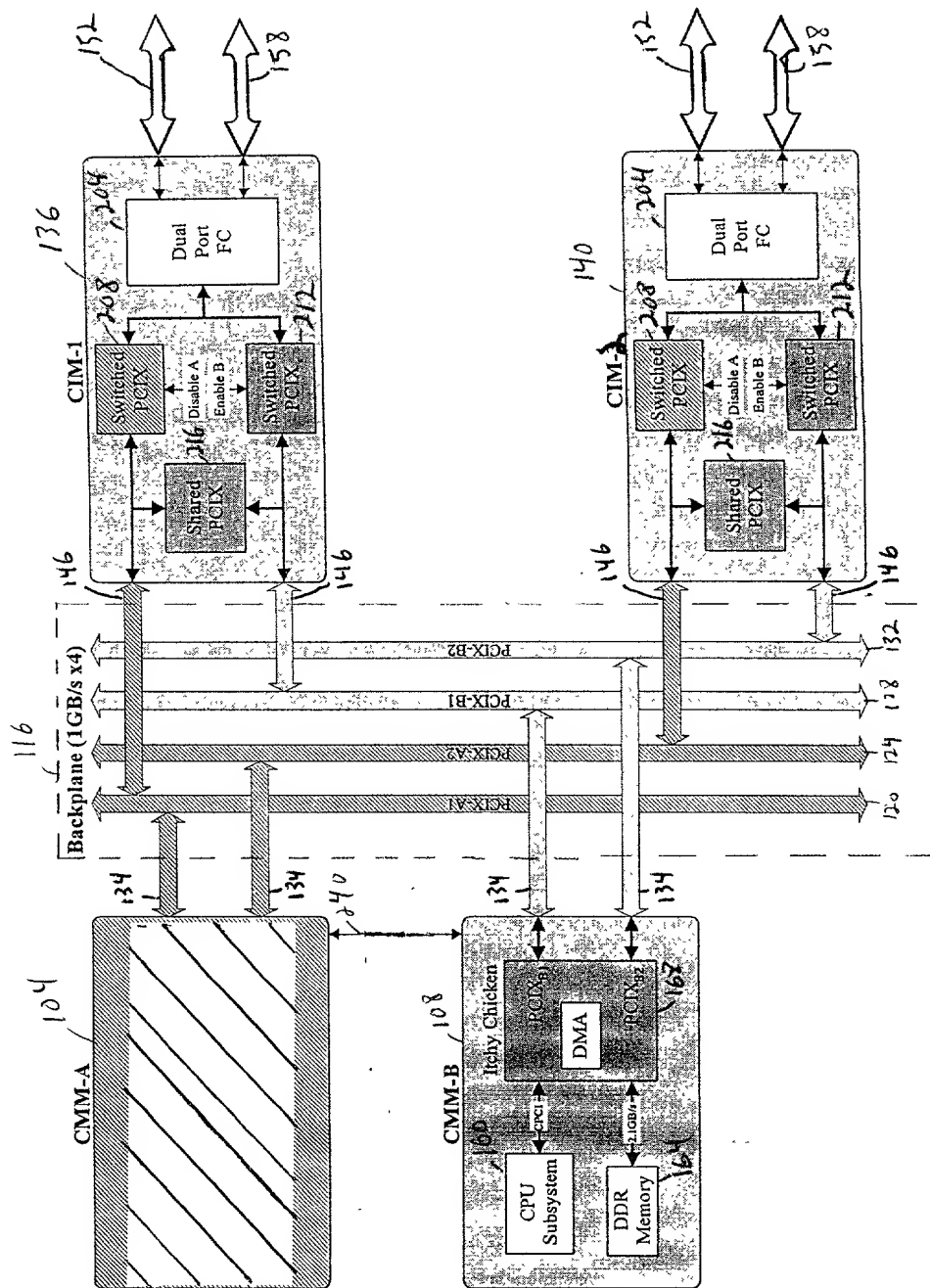
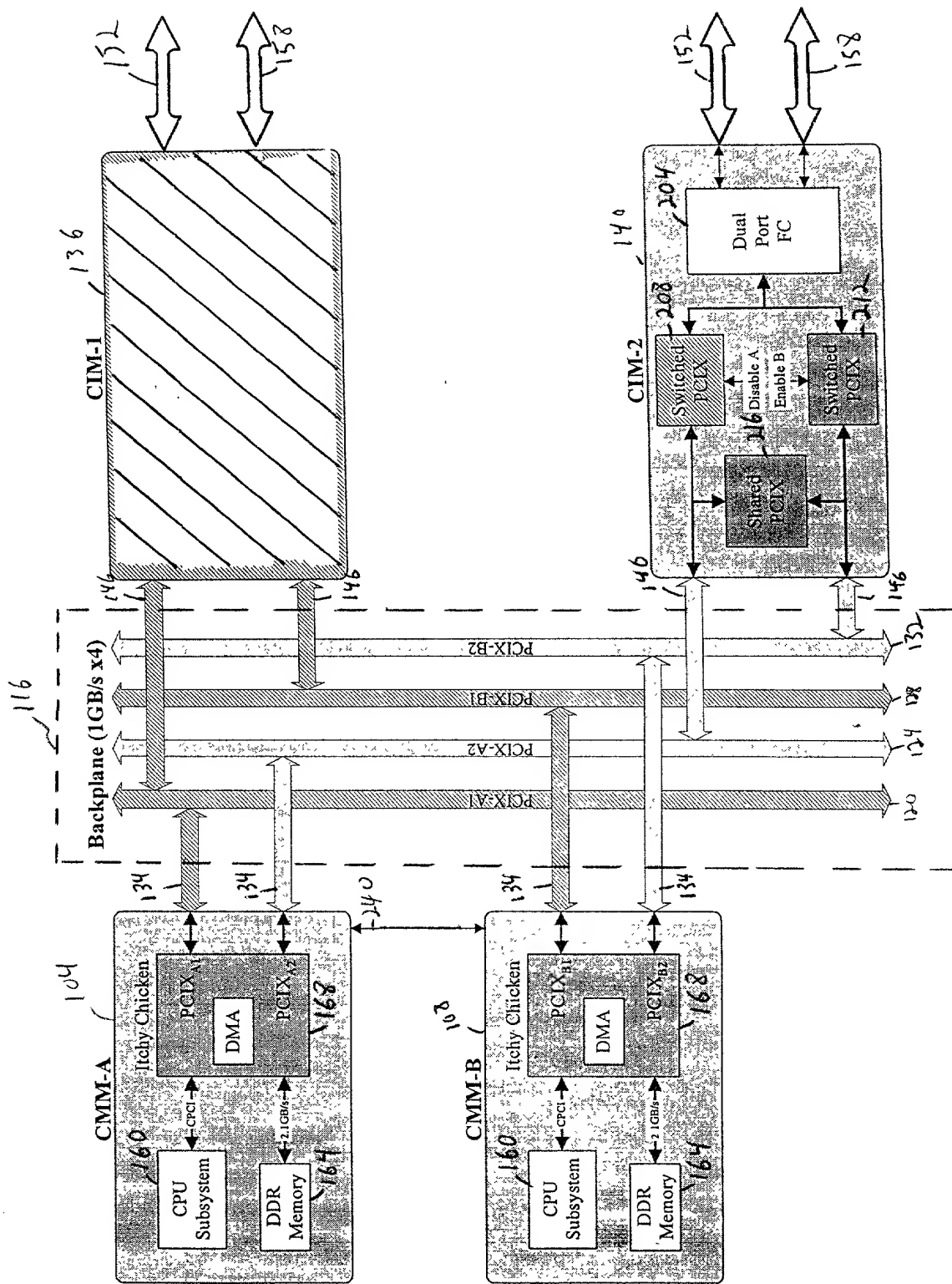
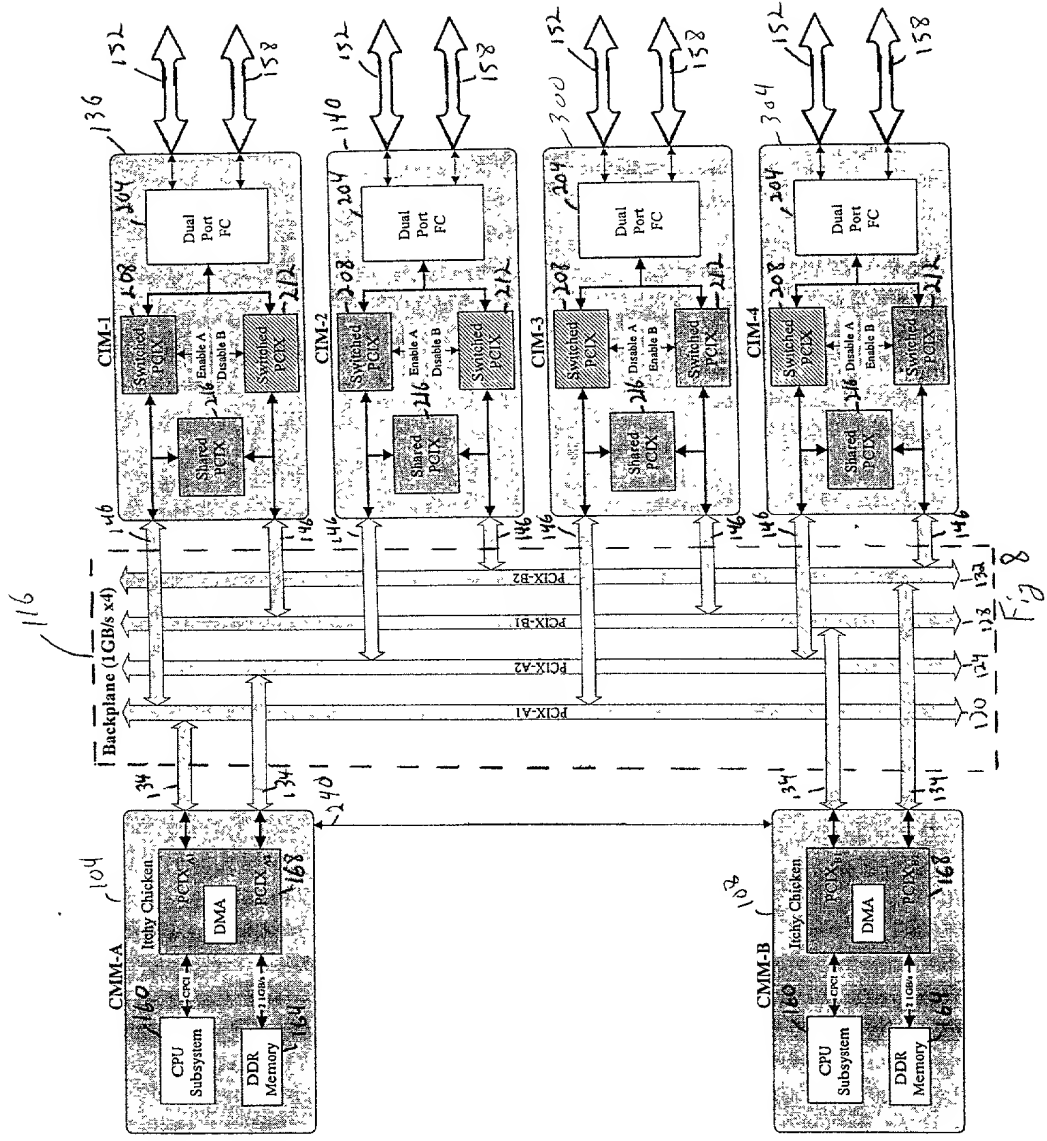


Fig. 6



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100

100b



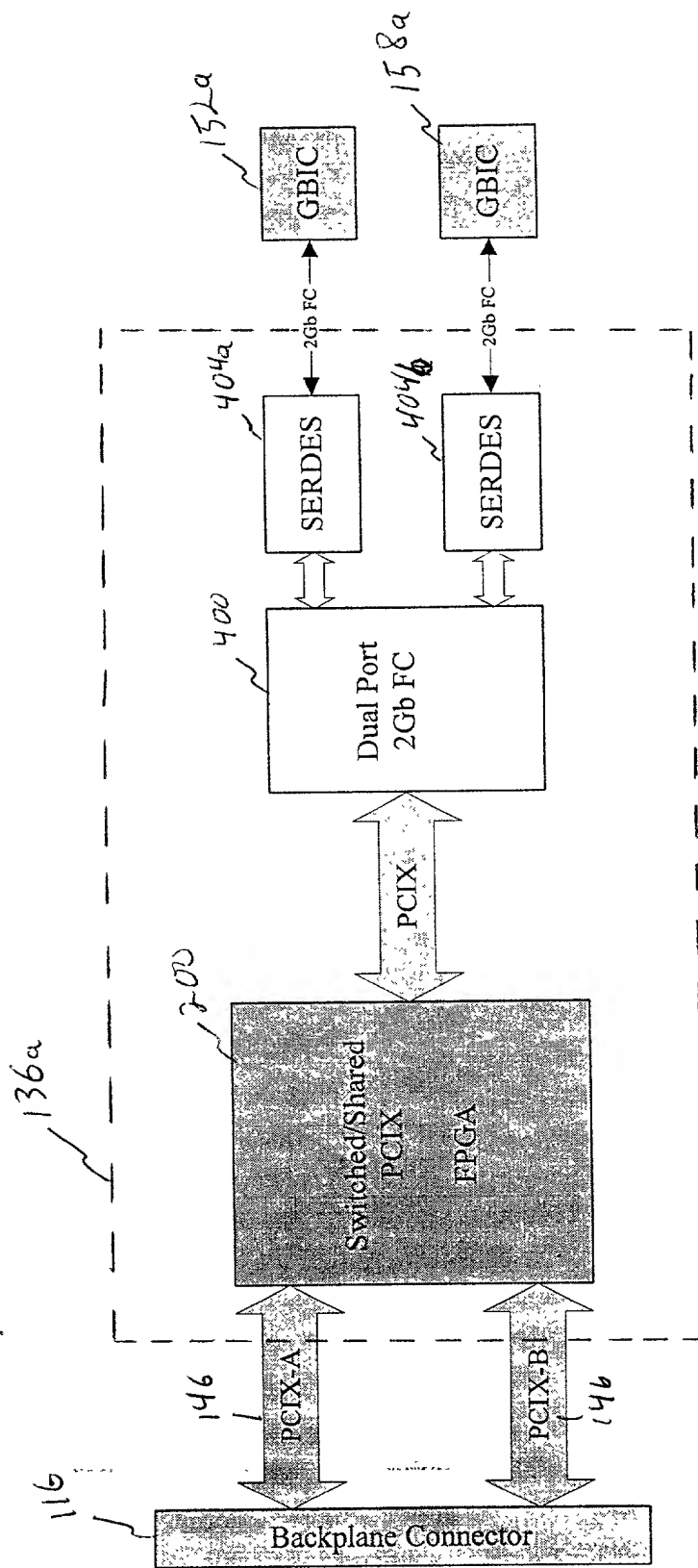


Fig 9

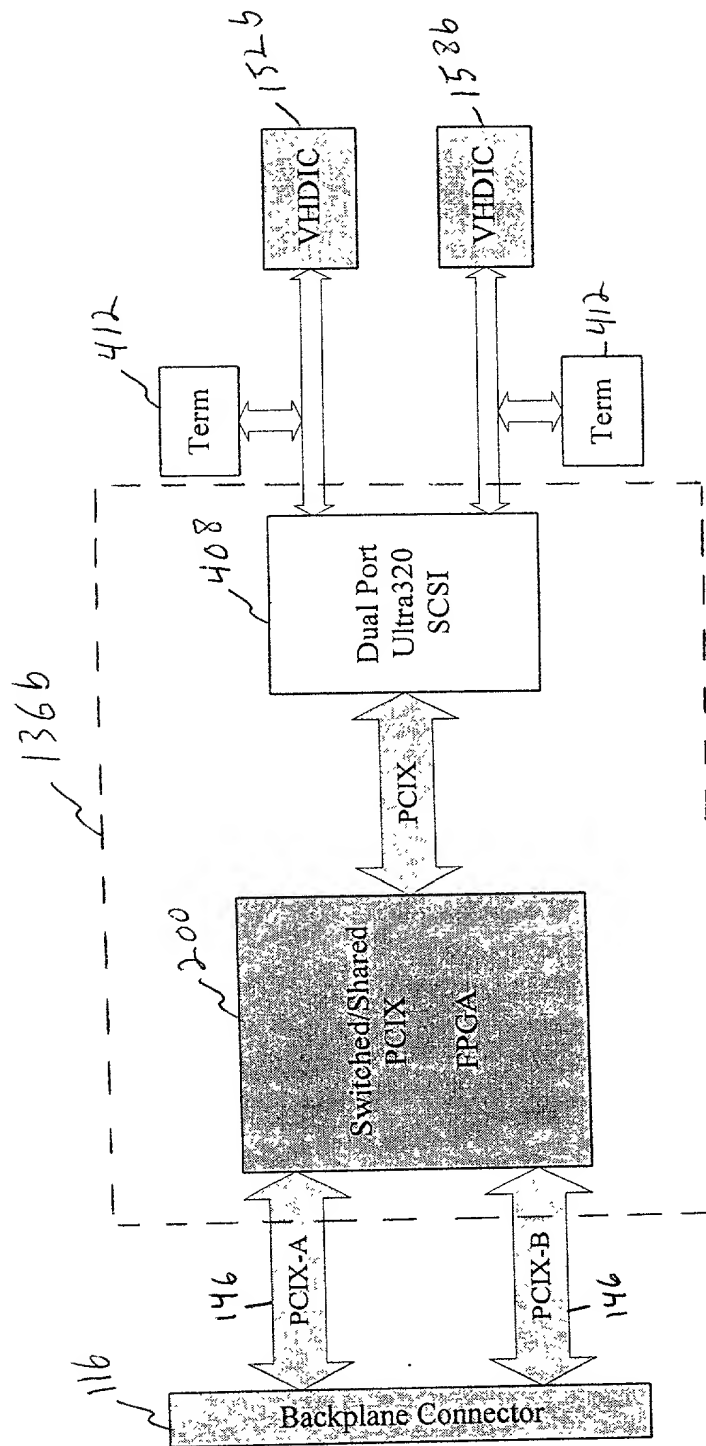


Fig 10

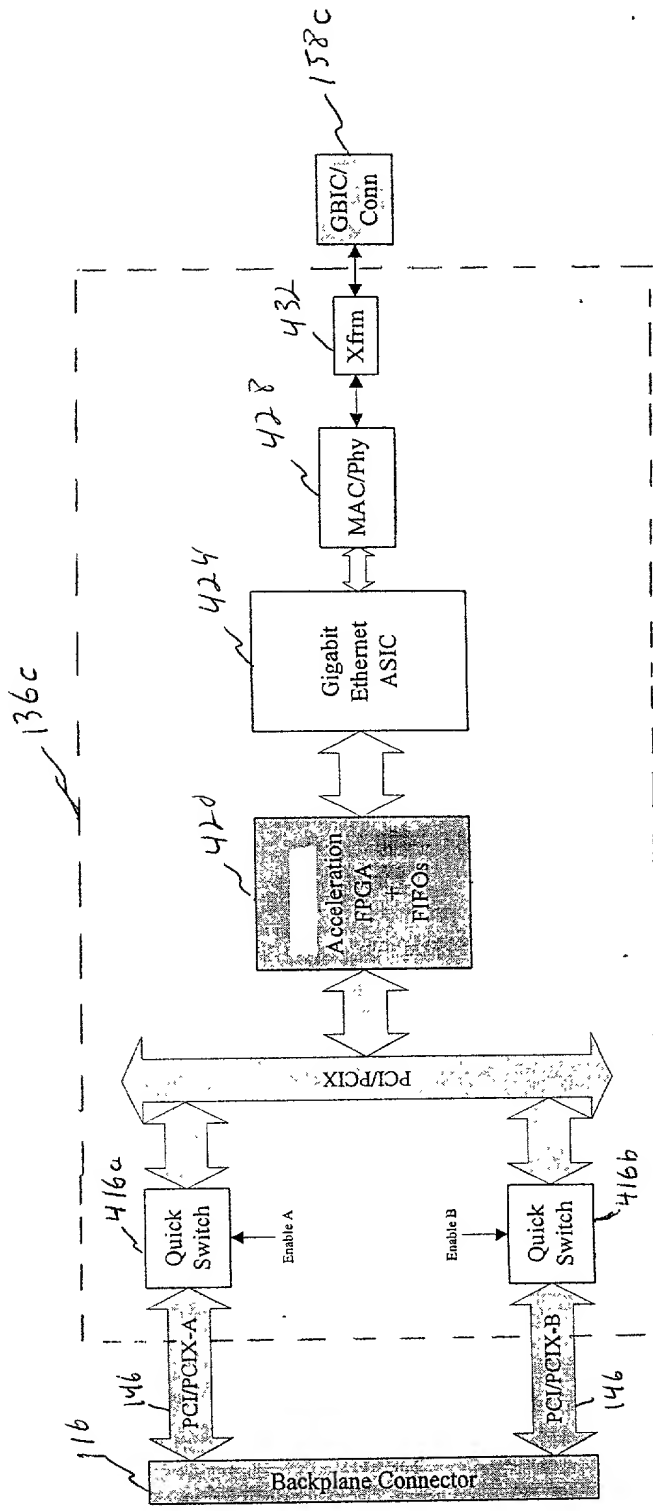


Fig. 11